Atty. Docket No. OPP031052US
Serial No: 10/728,699

Amendments to the Drawings

A new sheet of drawings is attached hereto, submitted as required by the Examiner. The new sheet includes drawings corresponding substantially to FIGS. 3d-e, but in which the remaining region of the LOCOS oxide layer(s) 15 is/are removed. Support for the new drawings can be found in FIGS. 3d-e and Claim 9 as originally filed, and in the specification as originally filed at p. 6, ll. 1-2, and p. 14, ll. 3-5. No new matter is introduced by the new sheet of drawings.

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Remarks

The present invention relates to a method of forming a trench in a semiconductor device. Claim 1 as amended recites:

- forming a sacrificial layer on a silicon wafer and selectively etching the sacrificial layer to form a LOCOS opening having a predetermined width;
- performing thermal oxidation on a portion of the silicon wafer exposed through the LOCOS opening to form a LOCOS oxide layer;
- etching the LOCOS oxide layer and the silicon wafer to a desired depth to form a trench, such that the LOCOS oxide layer is left remaining on the silicon wafer at an area corresponding to edges of the trench;
- removing the remaining region of the LOCOS oxide layer and forming a liner oxide layer in the trench; and
- forming an insulation layer such that the trench is filled with a material of the insulation layer.

U.S. Patent No. 5,910,018 to Jang (hereinafter, "Jang") does not anticipate the claimed invention, and U.S. Patent No. 6,184,105 to Liu et al. (hereinafter, "Liu et al.") neither teaches nor suggests the claimed invention.

The Rejection of Claims 1, 2, 5, 7, 11-15 and 21 under 35 U.S.C. §§ 102(b)

The rejection of claims 1, 2 5, 7, 11-15 and 21 under 35 U.S.C. § 102(b) as being anticipated by Jang is respectfully traversed.

Jang discloses a trench edge rounding method and structure for trench isolation (Title). In the process disclosed by Jang, a LOCOS oxide layer is etched such that no LOCOS oxide layer is left remaining on the silicon wafer (see, e.g., FIG. 5 and col. 3, ll. 17-25 of Jang and paragraph 4 on p. 2 of the Declaration of Young-Hun Seo, attached hereto).

For example, Jang shows a thick oxide layer 28 in FIG. 4, and discloses that "thick oxide layer 28 is grown using a thermal oxidation process" (col. 3, lines 17-19). Jang also explains that, in the process disclosed therein, "the length of lateral oxide extrusion (bird's beak) is short and has little effect on the effective diffusion (active) width" (col. 3, lines 23-25). These disclosure(s) by Jang clearly indicate to one skilled in the art of semiconductor processing and/or fabrication that thick oxide layer 28 is a LOCOS oxide layer. (See paragraphs 5-6 on p. 2 of the attached Declaration of Young-Hun Seo).

Jang clearly does not anticipate the present invention. For example, Jang states that "(t)he grown oxide layer 28 is then removed leaving a rounded isolation edge as shown in FIG. 5." (Col. 3, ll. 26-27 of Jang.) FIG. 5 of Jang shows complete removal of LOCOS oxide layer 28. (See also paragraph 7 on p. 2 of the attached Declaration of Young-Hun Seo).

Jang also shows in FIG. 7 an oxide layer 29, "formed thermally on the sides and bottom of trench 8 to anneal any trench etch damage and to encapsulate any defects that may occur." (Col. 4, lines 42-44.) In FIG. 7 of Jang, oxide layer 29 is clearly shown along an interface with silicon substrate 10, including in the locations where LOCOS oxide layer 28 was removed. These disclosure(s) recited in paragraph 8 above further indicate to one skilled in the art of semiconductor processing and/or fabrication that LOCOS oxide layer 28 is completely removed in the process of Jang. (See paragraphs 8-9 on pp. 2-3 of the attached Declaration of Young-Hun Seo).

In contrast, the present claim 1 recites etching the LOCOS oxide layer and the silicon wafer to a desired depth to form a trench, ***such that the LOCOS oxide layer is left remaining on the silicon wafer*** at an area corresponding to edges of the trench (see claim 1 as amended on March 16, 2005; emphasis added). Because Jang completely removes LOCOS oxide layer 28 before etching trench 8, Jang does not anticipate the present claims.

Therefore, this ground of rejection is unsustainable, and should be withdrawn.

The Rejection of Claims 3, 4, 6, 8 and 10 under 35 U.S.C. §§ 103(a)

The rejection of claims 3, 4, 6, 8 and 10 under 35 U.S.C. § 103(a) as being unpatentable over Liu et al. is respectfully traversed.

Liu et al. disclose a method of fabricating integrated circuit including field effect transistors (FET) having source and drain regions and a gate and with LOCOS isolation by selectively forming, after the FETs are fabricated, trench openings in the source or drain regions or in the LOCOS isolation to maximize the isolation in selected areas while reducing the amount of silicon used by the isolation (Abstract). As is shown in FIGS. 10-13, after etching the LOCOS oxide layer 37 and the silicon wafer 30 to form a trench 38a-b, Liu et al. do not remove the remaining region of the LOCOS oxide layer, as recited in the present claims. The Examiner appears to have acknowledged as much in the Office Action dated December 21, 2004 (see p. 7, the section entitled "Allowable Subject Matter," and claim 9 as originally filed), and by failing to point out where Liu et al. disclose or suggest removing the remaining region of the LOCOS oxide layer (see, e.g., p. 4 of the Office Action dated June 2, 2005). Therefore, this ground of rejection is not well understood by Applicant's undersigned representative.

In fact, the Office Action dated June 2, 2005 fails to point out where any of the limitations of claim 1 can be found in Liu et al. Since claim 3 depends on claim 1, claim 3 incorporates all of the limitations of claim 1 (see, e.g., 35 U.S.C. § 112, fourth paragraph). The burden is on the Examiner to point out with particularity where each limitation in the rejected claim can be found in a cited reference:

> [37 C.F.R.] § 1.104 Nature of examination.
>
> (c) Rejection of claims.
>
> (1) If the invention is not considered patentable, or not considered patentable as claimed, the claims, or those considered unpatentable will be rejected.
>
> (2) In rejecting claims for want of novelty or for obviousness, the examiner must cite the best references at his or her command. When a reference is complex or shows or describes inventions

> other than that claimed by the applicant, ***the particular part relied on must be designated*** as nearly as practicable. ***The pertinence of each reference,*** if not apparent, ***must be clearly explained*** and each rejected claim specified. (emphasis added)

If it is believed that Liu et al. renders unpatentable the present claims 3, 4, 6, 8 and 10, the Examiner must designate the particular parts of Liu et al. on which reliance is placed for disclosure of the limitations of claim 1, which each of the present claims 3, 4, 6, 8 and 10 incorporate. In the absence of such designation, Applicants respectfully request withdrawal of this ground of rejection.

However, for the sake of argument, even if Liu et al. discloses or suggests all of the limitations of the present claim 1, the present invention provides a significant advantage and/or improvement over the process of Liu et al. Liu et al. teach formation of a LOCOS oxide layer 37 and a trench 38a-b after formation of transistor source and drain terminals 16a-b (see, e.g., FIGS. 2-13 of Liu et al.). This process effectively reduces the active area of the transistor. In contrast, in the present invention, transistor gates and source and drain terminals may be formed after the LOCOS oxide layer has been etched and removed and the trench formed and filled (see claim 1). As a result, the present invention enables formation of transistor devices without necessarily reducing the active area of the transistors.

Consequently, the present claims are fully patentable over Liu et al.

The Objection to the Drawings

The objection to the drawings has been obviated in part by the new sheet of drawings attached hereto and in part by the above amendment to the specification. Support for the amendment to the specification can be found in the support for the new sheet of drawings and elsewhere in the specification at p. 13, l. 17-p. 14, l. 5. Thus, no new matter is introduced by the above amendment to the specification.

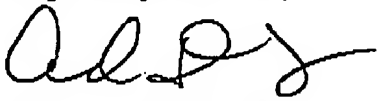
Atty. Docket No. OPP031052US
Serial No: 10/728,699

Conclusions

In view of the above amendments and remarks, all bases for objection and rejection are believed to be overcome, and the application is believed to be in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,



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